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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,968	12/19/2001	Steven G. Schmidt	87264.2560	1748

21834 7590 05/17/2006

BECK AND TYSVER P.L.L.C.
2900 THOMAS AVENUE SOUTH
SUITE 100
MINNEAPOLIS, MN 55416

EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,968	SCHMIDT, STEVEN G.	
	Examiner	Art Unit	
	Habte Mered	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/13/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4.5,7-14,16-18 and 23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4.5,7-14,16-18 and 23-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 2/13/2006 has been entered and fully considered.

2. Claims 2, 3, 6, 15, and 19-22 are cancelled.

3. Claims 1, 4, 5, 7-14, 16-18, and 23-35 are pending of which claims 23-35 are new.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 recites the limitation "the deferred header queue" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 4, 5, 8, and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Yamanaka et al (US 5, 619, 495), hereinafter referred to as Yamanaka, and Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant and Kadambi et al (US 6, 993, 027), hereinafter referred to as Kadambi.

Yamada teaches an ATM switch that is both input and output buffered. Yamada's system provides spare buffer to store data intended for an output that is

temporarily unable to accept data addressed to it. In Yamada's system Head Of Line Blocking is addressed by using spare buffers.

7. Regarding **claim 1**, Yamada teaches a buffer control apparatus **(See Figure 3, element 120)** in a buffered switch for controlling transmission of packets/frames of data with a deferred queue device to temporarily defer transmission of the packets/frames to a destination port which is unavailable to receive the packets/frames. **(Yamada in Figure 3 shows the deferred queue as cell buffers 140_2 and 140_3. See also Column 4, Lines 50-67.)** Yamada teaches a deferred queue containing entries having destination and buffer address information for data to be deferred, with entries for data addressed to multiple destination ports being intermingled within the deferred queue. **(See Column 5, Lines 1-15)**

Yamada fails to disclose that the buffers used have a buffer write module for writing packets/frames into the dual port buffer memory; a buffer read module for reading packets/frames of data from the dual port buffer memory.

Yamanaka discloses a cell switching system having buffer memories in which accesses of a plurality of cells can be implemented in one cell time.

Yamanaka teaches a system with a control buffer **(Figure 1, element 15)** and the buffers used are a dual port buffer memory for storing the packets/frames of data; a buffer write module **(Figure 1, element 16)** for writing packets/frames into the dual port buffer memory; a buffer read module **(Figure 1, element 19)** for reading packets/frames of data from the dual port buffer memory. **(Yamanaka further shows that in Figure 13 the buffer can be a dual port buffer memory. See also Column 16, Lines 20-30)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating dual port buffer memory with read and write module so that the read out and writing can be performed simultaneously to increase ports in the switch without increasing the access speed of the buffer memories. The motivation is a desire to increase the number of ports on Yamada's system without increasing the access speed of the buffer memories.

Yamada fails to teach a deferred header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

Merchant teaches a network switch configured for switching data packets across multiple ports and uses an internal memory to store frame headers for processing by decision-making logic.

Merchant discloses a deferred header queue device for storing frame information for packets/frames being deferred **(See Figures 4 and 5)**; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating deferred header queue with a header select logic to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to

increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

8. Regarding **claim 4**, Yamada teaches a buffer control apparatus, wherein the deferred queue device is in one of an Initial State, a Deferred State, and a Backup State and data received during the deferred state is analyzed for transmission or deferral after the deferred state has reviewed all entries in the deferred queue. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B)**

9. Regarding **claim 5**, Yamada teaches a buffer control apparatus, wherein the buffer control device further comprises: a backup queue device containing entries for data that arrived during the deferred state. **(Column 10, Lines 15-29)**

10. Regarding **claims 8 and 9**, Yamada teaches all aspects of the claimed invention but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating deferred header queue

with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

11. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yamanaka and Merchant as applied to claim 1 above, and further in view of Wallner et al (US 6, 442, 172), hereinafter referred to as Wallner.

The combination of Yamada, Yamanaka and Merchant teaches all aspects of the invention as set forth in the rejection of claim 1 but fails to disclose a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch, where the XOFF mask being a memory device having a bit associated with each possible destination port to receive data.

Wallner teaches input buffering and queue status based output control for a digital switch.

Wallner discloses a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch, where the XOFF mask being a memory device **(Figure 3, element 328)** having a bit associated with each possible destination port to receive data. **(Column 6, Lines 1-30 and see also Figure 3, element 328)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's, Yamanaka's and Merchant's system by incorporating XOFF mask. The motivation is a desire to increase switch processor speed in Yamada's system by using XOFF mask it will help to reduce switch traffic by cutting back on unnecessary feedback signaling within the switch.

12. **Claims 10-13 and 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant.

13. Regarding **claim 10**, Yamada teaches a deferred queue device for temporarily deferring transmission of packets/frames to a destination port in a buffered switch and means for periodically determining current status of all destination ports in the buffered switch. **(Yamada in Figure 3 shows the deferred queue as cell buffers 140_2 and 140_3. See also Column 4, Lines 50-67.)**

Yamada fails to teach a header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, which can now be sent to an available destination port.

Merchant discloses a header queue device for storing frame information for packets/frames being deferred; and header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, which can now be sent to an available destination port. . **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

14. Regarding **claim 11**, Yamada discloses a deferred queue device, wherein the deferred queue device can be in one of an Initial State, a Deferred State, and a Backup State. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B)**

15. Regarding **claim 12**, Yamada disclose a deferred queue device, further comprising: a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B. The spare cell buffers can be accessed in parallel.)**

16. Regarding **claim 13**, Yamada discloses a deferred queue device, further comprising: a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at least destination port. **(Yamada teaches that there can be several level of queues or spare cell buffers to handle the data that can be delivered to the busy output ports as indicated in Figure 4 A in steps 12 and steps 13 and step 24 in Figure 4B. The spare cell buffers can be accessed in parallel.)**

17. Regarding **claims 16 and 17**, Yamada teaches all aspects of the claimed invention as set forth in the rejection of claim 10 but fails to disclose a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

Merchant discloses a buffer control apparatus, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's and Yamanaka's system by incorporating deferred header queue with a header select logic, where stored information comprises frame header information and a starting address in the buffer memory for the packet/frame, to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing. The motivation is a desire

to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

18. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Merchant as applied to claim 10 above, and further in view of Wallner et al (US 6, 442, 172), hereinafter referred to as Wallner.

The combination of Yamada and Merchant teaches all aspects of the invention as set forth in the rejection of claim 10 but fails to disclose a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch, where the XOFF mask being a memory device having a bit associated with each possible destination port to receive data.

Wallner discloses a buffer control apparatus, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch, where the XOFF mask being a memory device **(Figure 3, element 328)** having a bit associated with each possible destination port to receive data. **(Column 6, Lines 1-30 and see also Figure 3, element 328)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's, Yamanaka's and Merchant's system by incorporating XOFF mask. The motivation is a desire to increase switch processor speed in Yamada's system by using XOFF mask it will help to reduce switch traffic by cutting back on unnecessary feedback signaling within the switch.

19. **Claim 18, 23, 24, 26, 27, 28 and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 5, 455, 820) in view of Kadambi et al (US 6, 993, 027), hereinafter referred to as Kadambi.

20. Regarding **claim 18**, Yamada discloses a method for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising the steps of: receiving a request for transmission of at least one packet/frame to the destination port **(Column 3, Lines 30-34 and also see Figure 1 item 30)**; determining whether the destination port is available to receive the at least one packet/frame **(Column 3, Lines 40-45 and item 50N in Figure 1. The destination port sends a signal indicating buffer occupancy level)**; deferring transmission of the at least one packet/frame when the destination port is not available to receive the at least one packet/frame **(Column 4, Lines 50-55 and S16 in Figure 4A)**; and repeating the above steps for a next packet/frame to be transmitted **(See Figures 4A and 4B)**.

21. Regarding **claims 26 and 35**, Yamada teaches a data switch **(Figure 1)** having a plurality of output ports **(Figure 1, 3001)**, each output port having a positive or negative transmission status **(Figure 3, 501 and 50N)**; the switch comprising: an input buffer receiving a plurality of data frames each associated with an output port **(Figure 3, 10)**; a mechanism at each input buffer to determine the transmission status of the output ports **(Figure 3, 501 and 50N)**; a deferred queue in which data for a plurality of different output ports having a negative transmission status is tracked**(Figure 3, 140_N)**; a backup queue in which newly received data is queued when data in the deferred queue is being processed**(Figure 3, 140_N)**; and a state

machine that enters a deferred state when an output port moves from a negative to a positive transmission status, the deferred state causing the data switch **(Figure 3, 120)**: to process data in the deferred queue so as to transmit to the associated output port that data which is addressed to an output port that now has a positive transmission status, to ensure that data in the deferred queue addressed to output ports that still have a negative transmission status remain in the deferred queue, and to place newly received data in the backup queue. **(See also Figure 4 and Column 4, Lines 50-55)**

22. Regarding **claim 27**, Yamada discloses a data switch, wherein the state switch enters a backup state when all data in the deferred queue is processed in the deferred state and data exists in the backup queue, the backup state causing the data switch to determine whether the data in the backup queue should be transmitted to its associated output ports or stored in the deferred queue based upon the transmission status of the data's associated output port. **(See also Figure 4 and Column 4, Lines 50-55 and Column 5, Lines 5-15)**

23. Regarding **claim 28,** Yamada discloses a data switch, wherein the switch moves from the backup state to the deferred state when an output port moves from the negative transmission state to the positive transmission status. **(See also Figure 4 and Column 4, Lines 50-55 and Column 5, Lines 5-15)**

24. Regarding **claim 29**, Yamada discloses a data switch, wherein the state machine enters a normal state when the deferred state is completed and no data exists in the backup queue, or when the backup state is completed and no port has

moved from the negative transmission state to the positive transmission state, and wherein the normal state causes the data switch to determine whether incoming data should be transmitted to the associated output port or queued on the deferred queue depending on the transmission status of the associated output port. **(See Column 5, Lines 15-25)**

25. With respect to **claims 18, 26-29, 34 and 35**, Yamada fails to disclose a state driven queue operation.

Kadambi teaches a method of sending a switch indicator to avoid frames being out of order in a network switch.

Kadambi discloses a state driven queue operation.

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating a state driven queue operation, the motivation being implementations based on a state machine are cheaper to maintain as they can be debugged easily during a maintenance operation.

26. Regarding **claim 23**, Yamada teaches a method, further comprising the steps of: periodically checking to determine if destination ports for data in the backup queue are available **(Figure 4b, Step 21)**; transmitting data to the destination ports when it is determined that the destination ports are available **(Figure 4b, Step 24)**; and placing the data in the deferred queue when it is determined that the destination ports are unavailable **(Figure 4b, Step 26)**.

27. Regarding **claim 24**, Yamada discloses a method wherein each frame/packet identifier is transmitted to the destination port based in the order in which the data was

received at the backup queue for the destination port. **(Yamada teaches that the deferred packet is transmitted from the spare cell buffers that serve as deferred queue to the destination port when the overflow clears and the buffers are FIFO. See Column 5, Lines 1-5)**

28. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Kadambi as applied to claim 18 above, and further in view of Merchant et al (US 6, 904, 043), hereinafter referred to as Merchant.

The combination of Yamada and Kadambi teaches all aspects of the invention as set forth in the rejection of claim 18 but fails to disclose a method, a header queue containing header information for all data in the queue, the header information containing destination information and a buffer address location indicating where the data resides in a buffer memory.

Merchant discloses disclose a method, a header queue containing header information for all data in the queue, the header information containing destination information and a buffer address location indicating where the data resides in a buffer memory. **(See Column 9, Lines 50-60 and Column 10, Lines 15-29; See also Figures 4 and 5)**

It would have been obvious to one having ordinary skill in the art at the time the invention is made to modify Yamada's system by incorporating header queue with the header information containing destination information and a buffer address location indicating where the data resides in a buffer memory to increase processor speed in the switch without sending the actual data from storage to the switch for re-processing.

The motivation is a desire to increase switch processor speed in Yamada's system and consequently increasing the number of ports it can handle.

29. Regarding **claim 34**, Yamada discloses a data switch of, wherein the data frames are selected from a group of frames comprising fixed length frames and packets, frames and packets having end of frame delimiters, and variable length data frames and packets. **(Yamada's switch is an ATM switch and any ATM switch meets this limitation)**

30. **Claims 30-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Kadambi as applied to claim 26 above, and further in view of Wallner et al (US 6, 442, 172), hereinafter referred to as Wallner.

30. Regarding **claim 30**, the combination of Yamada and Kadambi teaches all aspects of the invention as set forth in the rejection of claim 26 but fails to disclose a data switch, wherein the mechanisms to determine the transmission status of the output ports is an XOFF mask.

Wallner discloses a data switch of, wherein the mechanisms to determine the transmission status of the output ports is an XOFF mask. **(Column 6, Lines 1-10)**

31. Regarding **claim 31**, the combination of Yamada and Kadambi teaches all aspects of the invention as set forth in the rejection of claim 26 but fails to disclose a data switch, wherein the XOFF mask comprises a memory device having a bit associated with every output port, with each bit indicating either the ability or inability of the output port to receive data at a current time.

Wallner discloses a data switch, wherein the XOFF mask comprises a memory device **(Figure 3, element 328)** having a bit associated with every output port, with each bit indicating either the ability or inability of the output port to receive data at a current time. **(Column 6, Lines 1-30 and see also Figure 3, element 328)**

32. Regarding **claim 32**, the combination of Yamada and Kadambi teaches all aspects of the invention as set forth in the rejection of claim 26 but fails to disclose a data switch, wherein the XOFF mask is updated in real time except during the deferred state, during which time changes to the XOFF mask indicating a change of a port transmission status from negative to positive are delayed until all entries in the deferred queue have been analyzed.

Wallner discloses a data switch, wherein the XOFF mask is updated in real time except during the deferred state, during which time changes to the XOFF mask indicating a change of a port transmission status from negative to positive are delayed until all entries in the deferred queue have been analyzed. **(Column 6, Lines 30-35)**

33. Regarding **claim 33**, the combination of Yamada and Kadambi teaches all aspects of the invention as set forth in the rejection of claim 26 but fails to disclose a data switch, wherein the deferred state is reentered with an updated XOFF mask after all entries in the deferred queue are analyzed with an original XOFF mask if the change of a port transmission status from negative to positive occurs during the deferred state. **(Column 6, Lines 22-35)**

Wallner discloses a data switch, wherein the deferred state is reentered with an updated XOFF mask after all entries in the deferred queue are analyzed with an

original XOFF mask if the change of a port transmission status from negative to positive occurs during the deferred state. **(Column 6, Lines 22-35)**

34. With respect to **claims 30-33**, it would have been obvious to one having ordinary skill in the art at the time the invention is made to modify the combination of Yamada's, Yamanaka's and Kadambi's apparatus by incorporating XOFF mask, wherein the XOFF mask comprises a memory device having a bit associated with every output port, with each bit indicating either the ability or inability of the output port to receive data at a current time. The motivation is a desire to increase switch processor speed in Yamada's system by using XOFF mask it will help to reduce switch traffic by cutting back on unnecessary feedback signaling within the switch.

Response to Arguments

35. Applicant's arguments filed 2/13/2006 have been fully considered but they are not persuasive.

36. In the Remarks, on page 9 in the 3rd paragraph, Applicant argues that Yamada's spare buffer is allocated on a per output port basis and further argues that cells are simultaneously outputted from the spare buffer and the main buffer. Examiner respectfully disagrees with Applicant's conclusion. Referring to Figure 4A and Column 5, Lines 5-20 and 34-37 it is clear that the selected spare cell buffers are the designated deferred queue for the input buffer and cells are not transmitted simultaneously from the spare cell buffers serving as a deferred queue and the main buffer.

37. In the Remarks, on page 10 in the 1st paragraph, Applicant argues that Merchant does not teach deferred queue but teaches header queue. Examiner wants to

emphasize that deferred queue is taught by Yamada and Merchant is only introduced to teach header queue and therefore sees no contradiction.

Conclusion

38. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
05-15-2006

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600